



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,823	11/16/2001	Ameha Aklilu	RPS9 2001 0107	3066
47052	7590	06/08/2005	EXAMINER	
SAWYER LAW GROUP LLP			PATEL, NITIN C	
PO BOX 51418			ART UNIT	
PALO ALTO, CA 94303			PAPER NUMBER	
			2116	

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/990,823	Applicant(s) AKLILU ET AL.	
	Examiner Nitin C. Patel	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) 2,4,12,18,20,28 and 34 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,5-11,13-17,19,21-27,29-33,35 and 36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

RD

Art Unit: 2116

DETAILED ACTION

1. This is in responsive to RCE filed on 13 May 2005.
2. Claims 2, 4, 12, 18, 20, 28, and 34 have been cancelled.
3. Claims 1, 3, 5 – 11, 13 – 17, 19, 21 – 27, 29 – 33, and 35 – 36, are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
4. Claims 1, 3, 5 – 11, 13 – 17, 19, 21 – 27, 29 – 33, and 35 – 36, are rejected under 35 U.S.C. 103(a) as being unpatentable over Morisawa et al. [hereinafter as Morisawa], US 2002/0038328 A1, and further in view of Ebrahim, US Patent 5,878,264.
5. As to claims 1, 11, 17, 27, and 33, Morisawa discloses a system and method for reducing the boot time for a computer [para 0011, on page 1] comprising the steps of: when the computer is in powered down state [para 0031 on page 2, para 0039 on page

Art Unit: 2116

2 and 3]; supplying power [built-in battery is supplying power, fig. 1] to the computer disabling [by turning off] a plurality of input/output [I/O] devices coupled to the computer [para 0056, on page 4, S105 in fig. 5]; performing a boot process [performed by BIOS, para 0053 on page 4]; and placing the computer in a suspend to memory state [S3 state], wherein the steps (a) through (d) are performed before a user turns on the computer [para 0058, lines 1 – 2] [para 0050 - 0060 on page 4, fig. 5 – 6].

However, the teaching of setting flag [status flag] by a basic input/output system [BIOS] [para 0039 - 0046 on page 3, para 0068 on page 5, and para 0078 - 0080 on page 6] in Morisawa does not indicate that the computer is being booted from a powered down state.

Ebrahim teaches system with power sequence controller and method for processor reset procedure with an internal power-on reset flag check to determine the processor reset caused by the system's power being turned on [from a powered down state] including processor's prior state [from a powered down state] and decides warm boot or cold boot [col. 14, lines 6 – 55][col.2 through col. 10].

It would have been obvious to one of ordinary skill in art, having the teachings of Morisawa and Ebrahim before him at the time of invention was made, to modify a system and method for reducing the boot time for a computer as disclosed by Morisawa to include power sequence controller and the power-on set flag indicating cause of processor reset and prior state as taught by Ebrahim, in order to obtain a hardware based controller supporting software based transitioning of system's power state [col. 2, lines 3 – 24].

6. As to claims 3, and 19, Morisawa discloses supplying of power by supply AC outlet [para 0031 on page 2].
7. As to claims 5, 21, 30, and 34, Morisawa discloses a setting of activation flag F [enable/disable flag] in a register [enable/disable register, para 0078 - 0080 on page 6, fig. 4].
8. As to claims 6, 13, 22, 29, and 35 - 36, Morisawa discloses checking in storage register of memory [checking status flag, para 0068 on page 5] for different scenario of state transition [para 0039 on page 2 - 3, para 0050 - 0059 on page 4, para 0068 on page 5, fig. 4].
9. As to claims 7, and 23, Morisawa discloses that suspend to memory state is a S3 state [para 0050 on page 4].
10. As to claims 8, 14, 24, and 31, Morisawa discloses supplying power to the computer when computer is in the suspend to memory state (S3); resuming operation of an OS of the computer; checking a flag (state flag) by the OS, wherein the flag indicates whether or not the computer is being booted from a powered down state (S4) (inherent to a power save mode based on ACPI); enabling the plurality of I/O devices if the flag indicates that the computer is not being booted from the powered down state (S5); and operating the computer in a wake state [para 0050 - 0060 on page 4, para 0068 on page 5, para 0078 - 0080 on page 6].
11. As to claims 9 - 10, 15 - 16, 25 - 26 and 32, Morisawa discloses to place computer in suspend to memory state (S3) [fig. 5] and restoring it back to suspend state (S3) by manipulation start/stop switch [fig. 6].

12. **Examiner's note:** Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant.

Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

13. **Prior Art not relied upon:** Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am - 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2116

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
June 3, 2005


LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100